AMENDMENTS TO THE SPECIFICATION

A.B. 2/11/09

Please replace the paragraph beginning on page 6, line 6 with the following amended paragraph:

With the processor according to the present invention, a prescribed system instruction ~~in~~ is included in an application program and specifies the instruction set to be used. When the prescribed system instruction is decoded by a system instruction decoder and execution control is performed by the system instruction execution unit, the processor executes the read-in instruction using the processor function that corresponds to the instruction set used. The system instruction that specifies the instruction set used is executed using the system decoder and system instruction execution unit that are exclusively for the system instruction. Even if the instruction used is changed over, therefore, it is unnecessary to recognize the instruction set currently being used and changeover of the instruction set to be used can be performed with facility. Further, in a case where instruction sets having different processing performance orientations are included in the processor, the processing speed of overall processing can be raised by dynamically changing over to a performance-oriented instruction set suited to the particular~~ly~~ processing in accordance with the processing to be executed by the processor~~, and then.~~

A.B 2/11/09

Please replace the paragraph beginning on page 11, line 8 with the following amended paragraph:

The system LSI circuit in accordance with another aspect of the present invention is such that hardware resources can be shared among a plurality of instruction sets included in each processor, and therefore hardware resources can be exploited more effectively in comparison with a case where the system LSI circuit has independent processors separately for every instruction set. Further, since the instruction set used can be changed over dynamically

processor by processor, the processing performance of the system LSI circuit can be improved by selecting an instruction set in accordance with the processing required by the system LSI circuit.

A.B. 2/11/09 *Please replace the paragraph beginning on page 19, line ~~18~~ 10 with the following amended paragraph:*

Fig. 2 ~~is~~ illustrates a detailed example of the structure of processor 100 (1) shown in Fig. 1. As is the case with the processor 100 (1) shown in Fig. 2, each processor has a processor controller 110, a processing unit 130, an instruction memory controller 140 and a data memory controller 150. The components of each processor 100 will be described taking as an example the processor 100 (1) having the instruction set A and the instruction set B.

A.B 2/11/09 *Please replace the paragraph beginning on page ~~26~~ 25, line ~~7~~ 21 with the following amended paragraph:*

If a system instruction, in which it is specified that the operating mode is one where the instruction set used is the instruction set B and the clock frequency used is 100 MHz, is executed at time t1, the instruction set changeover unit 112 selects the side of instruction set B and the processor 100 (1) receives a 100-MHz clock signal from the clock bus 103b as the system clock. At this time, power having a value of voltage higher than that which prevailed prior to time t1 is supplied to the processor 100 (1) from the power-supply bus 103a in response to the increase in clock frequency. Owing to the changeover in instruction set used, the processor 100 (1) undergoes a mode change from the processor mode oriented toward ~~controll~~ control performance to the processor mode oriented toward signal processing performance and, hence, the execution of signal processing by the processor 100 (1) is speeded up.

A.B. 2/11/09 *Please replace the paragraph beginning on page 29, line ~~12~~ 10 with the following amended paragraph:*

The C-language description D5 for simulation obtained at the step S3, the debugging information D12 and machine-language instruction D13 obtained at step S5, and a test bench D14, which defines the peripheral environment inclusive of input/output signals for processor testing, are applied to an instruction-set simulator, and whether processor design includes an error is ~~recognized~~ checked (step S6). The instruction-set simulator debugs the processor configuration and the application program D10, estimates the time performance characteristic and power-dissipation characteristic, which are indicative of the processing performance of the processor, and outputs the time performance characteristic and power-dissipation characteristic as performance information D15.

A.B. 2/11/09 *Please replace the paragraph beginning on page ~~35~~ 34, line ~~1~~ 19 with the following amended paragraph:*

Fig. 7 illustrates an example of processing by the system LSI circuit of Figs. 5a, 5b and 5c in the form of a block diagram, and Fig. 8 illustrates the corresponding relationship between the processing by the system LSI circuit and the operating patterns. As shown in Fig. 7, the system LSI circuit has successively, as an application, receive filter processing for filtering received data, receive error correction processing for subjecting the filtered data to error correction, and receive-data expansion processing for expanding the error-corrected data, as well as communication control processing executed in parallel with control according to this processing.

A.B. 2/11/09 *Please replace the paragraph beginning on page 43, line ~~25~~ 10 with the following amended paragraph:*

The foregoing embodiments have been described with regard to an example in which the instruction set A and the instruction set B are composed of instruction sets having different processing performance orientations. However, a plurality of instruction sets included in a